Room-temperature detection of spin accumulation in silicon across Schottky tunnel barriers using a MOSFET structure

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Using a metal-oxide-semiconductor field effect transistor (MOSFET) structure with a high-quality CoFe/n^+-Si contact, we systematically study spin injection and spin accumulation in a nondegenerated Si channel with a doping density of $\sim 4.5 \times 10^{15} \mathrm{cm}^{-3}$ at room temperature. By applying the gate voltage (V_G) to the channel, we obtain sufficient bias currents (I_Bias) for creating spin accumulation in the channel and observe clear spin-accumulation signals even at room temperature. Whereas the magnitude of the spin signals is enhanced by increasing I_Bias, it is reduced by increasing V_G interestingly. These features can be understood within the framework of the conventional spin diffusion model. As a result, a room-temperature spin injection technique for the nondegenerated Si channel without using insulating tunnel barriers is established, which indicates a technological progress for Si-based spintronic applications with gate electrodes.

PACS numbers:

I. INTRODUCTION

Owing to the future intrinsic limits of the shrinking of silicon (Si)-based conventional complementary metal-oxide-semiconductor (CMOS) transistors, one should develop novel devices with additional functionalities. In particular, spin-based electronics (spintronics) are expected to markedly improve device performances because of its nonvolatility, reconstructibility, low power consumption, and so forth.[1–4] To combine the spintronics with Si-based semiconductor industry, it will become important to explore spintronic technologies compatible with Si.[5]

Fortunately, Si has been predicted to be a semiconductor with enhanced spin lifetime and spin transport length due to its low spin-orbit scattering and lattice inversion symmetry.[2] Focusing on these characteristics, Appelbaum *et al.* demonstrated spin transport across more than micrometer-order Si channels in spin-dependent ballistic hot-electron transport devices.[6, 7] Since they extracted lots of useful data at low temperatures, the phonon-induced spin relaxation in conduction band in Si was also discussed in theories.[8, 9] Recently, even at room temperature, electrical detections of spin accumulation with the three-terminal technique [10, 11] and of spin transport with the four-terminal technique[12] were demonstrated in lateral devices with degenerated channels.

For developing spin metal-oxide-semiconductor field-effect transistors (MOSFETs) suggested,[13, 14] there are still many issues. Source and drain (S/D) contacts with insulating tunnel barriers have so far been utilized for electrical spin injection techniques for Si devices[6, 7, 10–12, 15–19] because the tunnel barriers provide the solution of the impedance mismatch[20–22] and of the silicidation reaction[23] between ferromagnetic metal (FM) and semiconductors (SC). As a result, highly efficient spin injection into Si [23] and long-distance lateral spin transport in a nondegerated Si channel,[24] a Si/SiO$_2$ interface,[25, 26] and an undoped Si channel[27] were demonstrated in hot-electron transport devices with Al$_2$O$_3$ tunnel barriers at low temperatures. However, the use of the insulating tunnel barriers basically results in high contact resistance at the interface. For scalable spin MOSFETs with ultralow power consumption, reducing the parasitic resistance between S/D contacts will be strongly required. Thus, we aim to simultaneously realize highly efficient spin injection and low-resistance S/D contacts in Si-based devices.

To date, we have individually explored two important technologies, high-quality epitaxial growth of FM alloys including half-metallic Heusler alloys on Si[28–32] and spin injection into Si across the Schottky-tunnel barrier.[33–38] If we simultaneously realize the above two technologies in a single device, we will be able to open a way for highly efficient spin injection and detection with low parasitic resistance in the future. Recently, we developed electrical detection of spin-accumulation signals in Si with a metal-oxide-semiconductor field-effect transistor (MOSFET) structure with a high-quality CoFe/n^+-Si contact.[37] Interestingly, the spin signals can be modulated by applying the gate voltage even at room temperature.[37] However, the precise mechanism of the gate-modulated spin signals has not yet been discussed in detail.

In this paper, to discuss the gate-modulated spin signals in detail, we systematically study room-temperature spin injection, spin detection, and spin accumulation
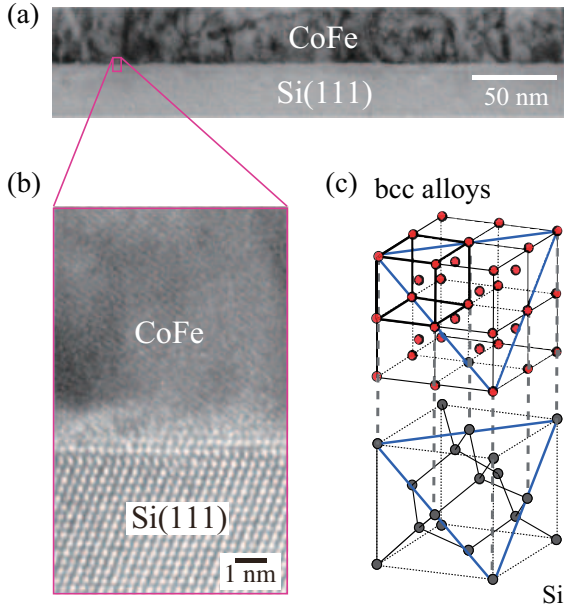
FIG. 1: (Color online) Cross-sectional (a) low-magnification and (b) high-resolution TEM images of CoFe/Si(111) interface. (c) Crystal structures of bcc-type FM and Si.

in non-degenerated Si channels using a metal-oxide-semiconductor field effect transistor (MOSFET) structure with a high-quality CoFe/n^+-Si contact. As a result, all the spin signals detected by the three-terminal Hanle-effect measurements for our device can quantitatively be understood within the framework of the standard spin diffusion model.[5] To precisely discuss the magnitude of spin signals, the correlation between tunnel spin polarization and resistivity of the channel with the change in the gate voltage should be considered in fabricated devices. This study shows a technological progress for Si-based spintronic applications with non-degenerated Si channels and without using insulating tunnel barriers.

II. HIGH-QUALITY SCHOTTKY TUNNEL CONTACT

Since the lattice mismatch between some of bcc-type FMs (0.564 $\sim$ 0.570 nm) and Si (0.543 nm) is less than 5%, we can expect to realize epitaxial growth of the FM films on Si. Until now, we have explored the growth of Heusler alloys and CoFe ones on Si(111).[28–31] As a result, the bcc-type FM films were successfully grown on Si at 60 $\sim$ 200 °C using low-temperature molecular beam epitaxy (MBE).[28–32]

Since CoFe alloys are conventional spin injector and detector, we will present a growth process in detail. First, an n-type Si wafer with (111) orientation was used as the substrate. After cleaning the substrates with an aqueous HF solution (HF : H_2O = 1 : 40), we conducted a heat treatment at 450 °C for 20 min in an

MBE chamber with a base pressure of 2×10^{-9} Torr. Prior to the growth of CoFe films, the substrate temperature was reduced to less than 60 °C. Using Knudsen cells, we co-evaporated Co and Fe, leading to precisely tuning the chemical composition.[30] During the growth, two-dimensional epitaxial growth was confirmed by the observation of reflection high-energy electron diffraction (RHEED) patterns.[30] Figure 1(a) shows a cross-sectional transmission electron microscopy (TEM) image of $Co_{45}Fe_{55}$ on Si(111). We can see almost no roughness at the CoFe/Si interface and no interfacial reaction layer at the entire region observed. A high-resolution TEM image near the interface is shown in Fig. 1(b). Almost atomically smooth interface can be seen and single crystalline CoFe alloys can be achieved. We have already examined the influence of atomic composition on the interfacial reaction for $Co_{100-x}Fe_x$ alloys. As a result, we obtained high-quality films on Si(111) from $x =$ 25 to 55.[30]

Why did we demonstrate such high-quality epitaxial growth without silicidation reactions ? We now consider the effect of crystal growth with atomically matched heterointerface at the (111) plane. Figure 1(c) illustrates the crystal structures for bcc-type FM alloys and Si. Looking at the (111) plane, denoted by triangles, there is very good atomic arrangement matching between FM and Si. We speculate that this special correlation between FM and Si can realize lowering crystallization energy. Actually, we have achieved high-quality epitaxial growth of Heusler alloys on Si.[28, 29, 31] This special condition can also be used for the growth of FM alloys on Ge.[39–44] Recently, room-temperature structural ordering of a Heusler alloy on Ge[45] and even the growth of Ge films on a FM alloy can be demonstrated surprisingly by using the (111) plane.[46]

III. SOI-MOSFET FOR SPIN INJECTION AND DETECTION

To fabricate a MOSFET structure with non-degenerated Si channels and Schottky-tunnel contacts, we utilized a CoFe alloy and a (111)-oriented Silicon On Insulator (SOI) substrate. Using low-temperature MBE (LT-MBE) techniques described above, the CoFe epitaxial layers with a thickness of $\sim$ 10 nm were grown on (111)-SOI at $\sim$ 25 °C,[30] where the thicknesses of the SOI and buried oxide (BOX) layers were about 75 and 200 nm, respectively. Since the doping density (P) of the SOI layer is $\sim 4.5 \times 10^{15}$cm^{-3} (1 $\sim$ 5 Ωcm) at room temperature, the used Si channel is a non-degenerated semiconductor. To obtain tunneling conduction of electrons for spin injection and detection, n^+-Si layer was inserted between CoFe and SOI by a combination of the Si epitaxy using an MBE process with an Sb δ-doping technique,[47, 48] where the doping density of Sb atoms is $\sim 1 \times 10^{19}$cm^{-3}.

The Sb δ-doped n^+-Si layer on the channel region
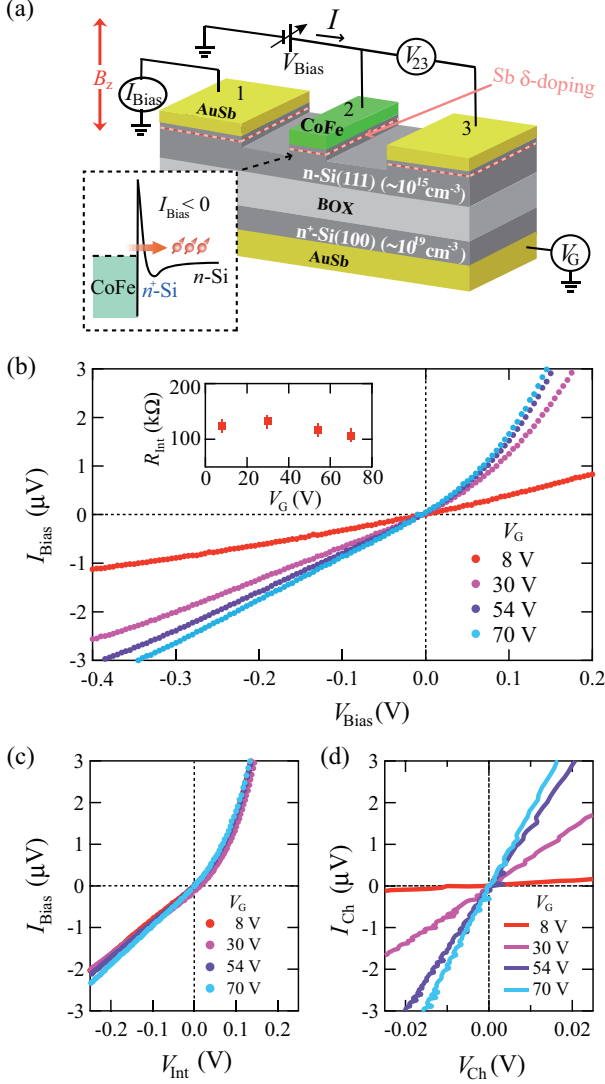
FIG. 2: (Color online) (a) Schematic diagram of a Si-MOSFET structure with a CoFe/n^+-Si Schottky-tunnel contact fabricated. (b) $I_{Bias}-V_{Bias}$ characteristics for various V_G at room temperature. The inset shows R_{Int} vs V_G at $V_{Int}=$ -0.2 V. (c) $I_{Bias}-V_{Int}$ and (d) $I_{Ch}-V_{Ch}$ curves for various V_G at room temperature.

was removed by the Ar$^+$ ion milling. An ohmic contact (AuSb) for backside heavily doped Si was formed at less than 300 °C. Conventional processes with electron-beam lithography, Ar$^+$ ion milling, and reactive ion etching were used to fabricate three-terminal lateral devices with a backside gate electrode, illustrated in Fig. 2(a). The CoFe/n^+-Si contact (contact 2) and AuSb ohmic contacts (contact 1 and 3) have lateral dimensions of 1×100 μm^2 and 100×100 μm^2, respectively. The distance between the contacts 2 and 1 or 3 is ~ 30 μm.

Using this device structure, we firstly confirm a MOSFET operation at room temperature. With increasing gate voltage (V_G), the bias current (I_{Bias}) value gradually increases with respect to the bias voltage (V_{Bias})
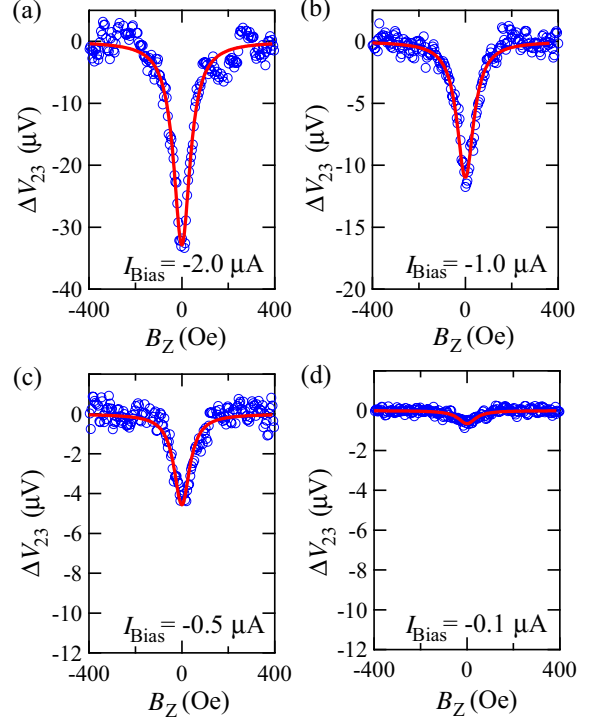

FIG. 3: (Color online) Room-temperature spin accumulation signals measured at $V_G = 8.0$ V for various $I_{Bias} =$ (a) -2.0, (b) -1.0, (c) -0.5, and (d) -0.1 μA. The red curves are fitting results by the Lorentzian function.

[Fig. 2(b)]. This means that the conduction channel is formed from the vicinity of the interface between SOI and BOX by the V_G applications, clearly indicating that this device can operate as a MOSFET. Figure 2(c) show $I_{Bias}-V_{Int}$ curves for various V_G, where V_{Int} is the bias voltage applied to the CoFe/n^+-Si interface. Here V_{Int} is V_{23} in the three-terminal measurement. We note that there are almost no changes in the $I_{Bias}-V_{Int}$ curves despite applying V_G. Reflecting this feature, we find almost constant interface resistance (R_{Int}) values (105 $\sim$ 120 kΩ), being independent on V_G, in the inset of Fig. 2(b). The resistance area product of the CoFe/n^+-Si contact is estimated to be $\sim 10^7$ $\Omega\mu m^2$, which is sufficient large value for the spin injection and detection in nondegenerated Si channels with a carrier density of $\sim 10^{15} cm^{-3}$.[5, 21]

We also show $I_{Ch}-V_{Ch}$ curves for various V_G, where V_{Ch} is the bias voltages applied to the Si channel. Here V_{Ch} is the subtracted value from V_{Bias} to V_{23}. Contrary to Fig. 2(c), we can clearly see the significant modulation of I_{Ch} values by applying V_G. That is, we can recognize that the $I_{Bias}-V_{Bias}$ characteristic shown in Fig. 2(b) is largely dominated by the change in the characteristics of the Si channel. By applying V_G, we can obtain sufficient large current flows of several μA for spin injection from the CoFe contact to the Si channel.

IV. SPIN ACCUMULATION IN NONDEGENERATED SI

The three-terminal Hanle measurements were performed by a dc method with the current-voltage configuration shown in Fig. 2(a) at room temperature, where a small magnetic field perpendicular to the plane, B_Z, was applied after the magnetic moment of the contact 2 aligned parallel to the plane along the long axis of the contact. Figures 3(a)-(d) show $\Delta V_{23}-B_Z$ curves for $V_G =$ 8.0 V at various I_{Bias} = -2.0, -1.0, -0.5, and -0.1 μA, respectively, at room temperature, where a quadratic background voltage depending on B_Z is subtracted from the raw data. Here in this condition ($I_{Bias} < 0$) the electrons are injected from the spin-polarized states of CoFe into the conduction band of Si, as shown in Fig. 2(a). When B_Z increases from zero to $\pm$200 Oe, clear ΔV_{23} changes are observed for all I_{Bias} even at room temperature. The presence of the changes in ΔV_{23} is caused by the depolarization of the accumulated spins.[5] It should be noted that the magnitude of ΔV_{23} reaches ~ 33 μV at I_{Bias} = -2.0 μA, showing the resistance change in more than 15 Ω. With decreasing I_{Bias}, the magnitude of ΔV_{23} is markedly reduced. This feature is consistent with the decrease in the injection of spin-polarized electrons.

We also examine $\Delta V_{23}-B_Z$ curves for various V_G at a constant I_{Bias} of -2.0 μA. Because of the large channel resistance and the presence of the large electrical noise, we could not obtain Hanle-like shapes in $V_G < 8.0$ V. At $V_G = 30$ V, a relatively large change in ΔV_{23} of ~ 29 μV is obtained in Fig. 4(a), but we find that the magnitude of ΔV_{23}, $|\Delta V_{23}|$, is slightly reduced from ~ 33 to ~ 29 μV by applying V_G from 8.0 to 30 V. Surprisingly, the magnitude of ΔV_{23} is further decreased to $\sim$12 μV when the gate voltage is further applied up to $V_G = 70$ V in Fig. 4(b). Figure 4(c) displays $|\Delta V_{23}|$ vs V_G for various I_{Bias} at room temperature. With increasing V_G, $|\Delta V_{23}|$ is clearly decreased for each I_{Bias}. When we note again the V_G dependence of R_{Int} in the inset of Fig. 2(b), we find that the change of R_{Int} with V_G is not related to that of $|\Delta V_{23}|$. Thus, we focus on large changes in the characteristics of the Si channel, as shown in Fig. 2(d). We will discuss the detailed mechanism of the decrease in $|\Delta V_{23}|$ with increasing V_G later.

V. SPIN LIFETIME VS GATE VOLTAGE

The lower limit of spin lifetime (τ_S) can be extracted from the obtained Hanle-effect curves.[5] By using the Lorentzian function, $\Delta V_{23}(B_Z) = \Delta V_{23}(0)/[1+(\omega_L\tau_S)^2]$,[10] the width of the Hanle-effect curve can be regarded as the value of τ_S, where $\omega_L = g\mu_B B_Z/\hbar$ is the Lamor frequency, g is the electron g-factor ($g = 2$), μ_B is the Bohr magneton. The fitting results were denoted by the red solid curves in Figs. 3(a)-(d) and Figs. 4(a) and 4(b). Figure 5 shows τ_S versus V_G at room temperature, together with the change in ρ_{Si}

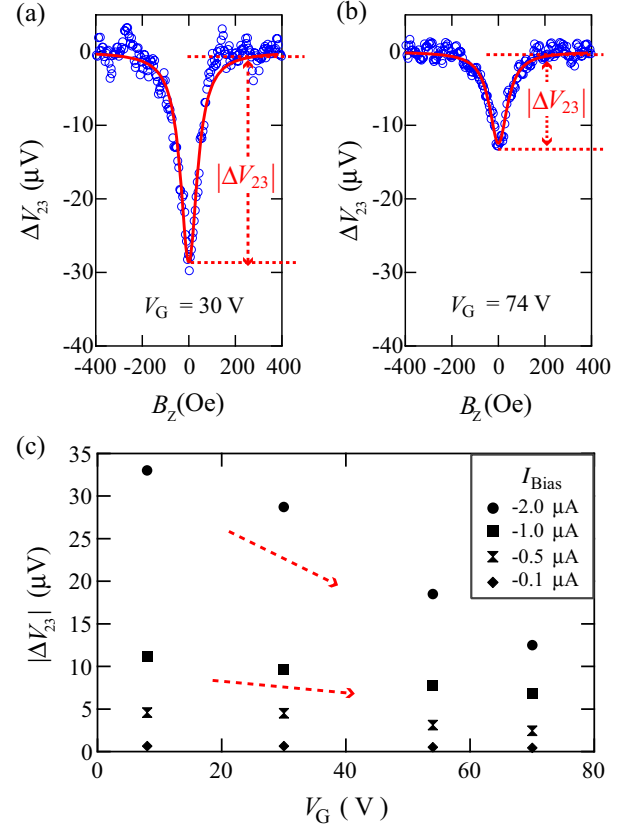FIG. 4: (Color online) Room-temperature spin accumulation signals measured at (a) $V_G = 30$ V and (b) = 74 V at I_{Bias} = -2.0 μA. The red curves are fitting results by the Lorentzian function. (c) $|\Delta V_{23}|$ vs V_G at various I_{Bias} at room temperature.

with V_G. The estimated τ_S values are ranging from 1.0 to 2.0 nsec. In general, the estimated τ_S values are affected by these doping elements and its doping density.[5] For our devices, the spin accumulation is created in the P-doped channel beneath the contact with Sb δ-doped interface. It should be noted that τ_S is almost constant whereas ρ_{Si} largely changes more than one ordered of magnitude. This means that there is almost no correlation between τ_S and the change of the carrier density induced by V_G in the Si channel, largely different from the dependence of the impurity doping density on the τ_S value presented in previous works.[5, 10, 11] Therefore, at room temperature, we can regard the spin diffusion length (λ_{Si}) as almost constant value for our devices. Assuming $D \sim 40$ cm^{2}s^{-1} ($n \sim 10^{15}$cm^{-3}),[50] we can also obtain $\lambda_{Si} \sim 2.3$ μm at room temperature by using the relationship of $\lambda_N = \sqrt{D\tau_S}$ ($\tau_S \sim 1.3$ nsec).

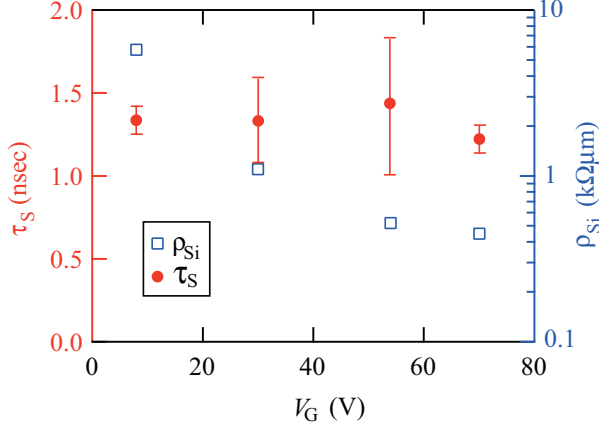FIG. 5: (Color online) Spin lifetime (τ_S) and channel resistivity (ρ_Si) as a function of V_G at room temperature.

VI. MAGNITUDE OF SPIN-ACCUMULATION SIGNAL

When the current density (J) is assumed to be $|I_\mathrm{Bias}|/A$, where A is contact area ($100\ \mu\mathrm{m}^2$) of this device, the experimental spin resistance area-product (spin-RA) can roughly be estimated to be $\frac{|\Delta V_{23}|}{J}$ ($\Omega\mu m^2$). For example, the spin-RA at $V_\mathrm{G} = 8.0$ V and $I_\mathrm{Bias} = -\ 2.0$ μA is roughly ~ 1.65 k$\Omega\mu\mathrm{m}^2$. On the basis of the simple spin diffusion model,[21, 22] the theoretical spin-RA can be expressed as follows.[5]

$$\text{Spin-}RA = P^2 \times \lambda_\mathrm{Si} \times \rho_\mathrm{Si} \times \frac{\lambda_\mathrm{Si}}{d}, \qquad (1)$$

where P is the tunnel spin polarization, λ_Si and ρ_Si are the spin diffusion length and resistivity of the Si channel used, respectively. $\frac{\lambda_\mathrm{Si}}{d}$ is the geometrical factor of our devices,[5] where d is the channel thickness ($= 0.075$ μm). By comparing Eq.(1) with experimental spin-RA values, we can roughly estimate experimental P values. Here $\lambda_\mathrm{Si} = 2.3$ μm is assumed and ρ_Si values at various V_G are experimentally obtained in Fig. 5. In Fig. 6 we summarize the estimated P as a function of V_G, together with the experimental spin-RA at $I_\mathrm{Bias} = -\ 2.0$ μA. The estimated P values are less than 0.2 for all V_G. Recently, the room-temperature spin polarization of epitaxial CoFe films on Si(111) was estimated to be less than 0.25 by nonlocal spin-signal measurements using metallic lateral spin valves.[49] The experimental tunnel spin polarization extracted here are smaller than $P = 0.25$. From these considerations, at least, our experimental results can be understood within the framework of the theoretical spin diffusion model.[21, 22] We note that $P \sim 0.065$ at $V_\mathrm{G} = 8.0$ V is relatively small compared with $P \sim 0.15$ at other V_G.

As shown in Fig. 5, ρ_Si at $V_\mathrm{G} = 8.0$ V is one order of magnitude larger than those at other V_G. Since the resistance area product for our device is almost constant
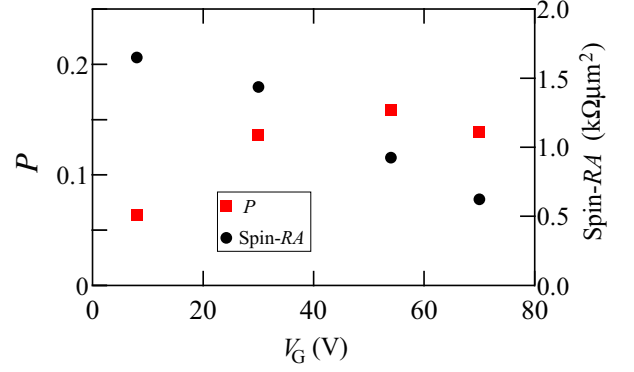

FIG. 6: (Color online) The estimated tunnel spin polarization (P) and the spin RA as a function of V_G at room temperature.

($\sim 10^7$ $\Omega\mu\mathrm{m}^2$) despite changing V_G, we can understand that the spin injection efficiency for $V_\mathrm{G} = 8.0$ V is relatively low compared with that for other V_G due to influence of the impedance mismatch problem.[5, 20–22] We note that $|\Delta V_{23}|$ is linearly reduced in Fig. 4(c) despite the logarithmic decrease in ρ_Si in Fig. 5. Although we can tentatively speculate that the change in $|\Delta V_{23}|$ with V_G originates from the change in ρ_Si from Eq.(1), the correlation between P and ρ_Si with changing V_G should be considered. From $V_\mathrm{G} = 8$ to 30 V, P is enhanced from 0.065 to 0.14, leading to the enhancement in $|\Delta V_{23}|$, whereas ρ_Si is logarithmically reduced, giving rise to the decrease in $|\Delta V_{23}|$. In this case, since the change in ρ_Si is much larger that in P from $V_\mathrm{G} = 8$ to 74 V, the change in $|\Delta V_{23}|$ is dominantly affected by the decrease in ρ_Si. Phenomenologically, even if the same I_Bias is used for spin injection into the Si channel, the density of state in Si at the Fermi level can be varied by the application of V_G. As a result, the magnitude of spin accumulation ($\Delta\mu$) can be reduced.[37]

We finally comment on a possible method to enhance the magnitude of spin signals at room temperature. Although relatively small P of less than 0.2 has been obtained in this study (Fig. 6), an intrinsic spin polarization of our epitaxial CoFe electrodes is less than 0.25 at room temperature.[49] Thus, we can regard the spin injection efficiency as relatively high. Considering Eq.(1), we need to enhance P value for the low-power consumption devices. Since we have already demonstrated highly ordered Heusler alloys, which have relatively high spin polarization intrinsically,[49, 51, 52], grown on Si with keeping high-quality heterointerfaces, we will use these spin injectors and detectors to enhance the room-temperature spin signals for device applications. If we achieve nearly half-metallic spin injectors on Si, we would not have to consider the insertion of the relatively high interface resistance between Si and spin injector.[19, 21, 22, 51] As a result, the low parasitic resistance S/D contacts may simultaneously be realized. For spin transport, the influence of Schottky barriers

VII. CONCLUSIONS

We have studied room-temperature detection of spin accumulation in a nondegenerated Si channel with a doping density of $\sim 10^{15} \text{cm}^{-3}$ using a MOSFET structure with a CoFe/n^+-Si contact. The observed spin accumulation signals can be modulated by the application of the gate voltage. We can interpret that the change in the spin-accumulation signals is attributed dominantly to the change in the resistivity of the Si channel, indicating reliable evidence for the spin injection into the nondegenerated Si channel at room temperature. We established a room-temperature spin injection technique for the nonde-generated Si channel without insulating tunnel barriers, indicating a technological progress for Si-based spintronic applications with gate electrodes.

[1] S. A. Wolf, D. D. Awschalom, R. A. Buhrman, J. M. Daughton, S. von Molnár, M. L. Roukes, A. Y. Chtchelkanova and D. M. Treger, Science **294**, 1488 (2001).
[2] I. Žutić, J. Fabian, and S. Das Sarma, Rev. Mod. Phys. **76**, 323 (2004).
[3] K. Takanashi, Jpn. J. Appl. Phys. **49**, 110001 (2010).
[4] T. Taniyama, E. Wada, M. Itoh and M. Yamaguchi, NPG Asia Mater. **3** 65 (2011).
[5] R. Jansen, Nature Mat. **11**, 400 (2012); R. Jansen, S. P. Dash, S. Sharma, and B. C. Min, Semicond. Sci. Technol. **27**, 083001 (2012).
[6] I. Appelbaum, B. Huang, and D. J. Monsma, Nature **447**, 295 (2007).
[7] I. Appelbaum, Phil. Trans. R. Soc. A **369**, 3554 (2011).
[8] J. L. Cheng, M. W. Wu, and J. Fabian, Phys. Rev. Lett. **104**, 016601 (2010).
[9] Y. Song and H. Dery, Phys. Rev. B **86**, 085201 (2012).
[10] S. P. Dash, S. Sharma, R. S. Patel, M. P. Jong, and R. Jansen, Nature (London) **462**, 491 (2009).
[11] C. H. Li, O. M. J. van't Erve, and B. T. Jonker, Nat. Commun. **2**, 245 (2011).
[12] T. Suzuki, T. Sasaki, T. Oikawa, M. Shiraishi, Y. Suzuki, and K. Noguchi, Appl. Phys. Express **4**, 023003 (2011).
[13] S. Sugahara and M. Tanaka, Appl. Phys. Lett. **84**, 2307 (2004).
[14] H. Dery, P. Dalal, Ł. Cywiński, and L. J. Sham, Nature (London) **447**, 573 (2007).
[15] O. M. J. van't Erve, A. T. Hanbicki, M. Holub, C. H. Li, C. Awo-Affouda, P. E. Thompson, and B. T. Jonker, Appl. Phys. Lett. **91**, 212109 (2007).
[16] R. Jansen, B. C. Min, S. P. Dash, S. Sharma, G. Kioseoglou, A. T. Hanbicki, O. M. J. vanft Erve, P. E. Thompson, and B. T. Jonker, Phys. Rev. B **82**, 241305(R) (2010).
[17] K. R. Jeon, B. C. Min, I. J. Shin, C. Y. Park, H. S. Lee, Y. H. Jo, and S. C. Shin, Appl. Phys. Lett. **98**, 262102 (2011).
[18] T. Sasaki, T. Oikawa, M. Shiraishi, Y. Suzuki, and K. Noguchi, Appl. Phys. Lett. **98**, 012508 (2011).
[19] M. Ishikawa, H. Sugiyama, T. Inokuchi, K. Hamaya, and Y. Saito, Appl. Phys. Lett. **100**, 252404 (2012).
[20] E. I, Rashba, Phys. Rev. B **62**, R16267 (2000).
[21] A. Fert and H. Jaffrès, Phys. Rev. B **64**, 184420 (2001).
[22] S. Takahashi and S. Maekawa, Phys. Rev. B **67**, 052406 (2003).
[23] B. Huang, L. Zhao, D. J. Monsma, and I. Appelbaum, Appl. Phys. Lett. **91**, 052501 (2007).
[24] H. J. Jang, J. Xu, J. Li, B. Huang, and I. Appelbaum, Phys. Rev. B **78**, 165329 (2008).
[25] H. J. Jang and I. Appelbaum, Phys. Rev. Lett. **103**, 117202 (2009).
[26] J. Li and I. Appelbaum, Phys. Rev. B **84**, 165318 (2011).
[27] J. Li and I. Appelbaum, Appl. Phys. Lett. **100**, 162408 (2012).
[28] K. Hamaya, K. Ueda, Y. Kishi, Y. Ando, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **93** 132117 (2008).
[29] S. Yamada, K. Hamaya, K. Yamamoto, T. Murakami, K. Mibu, and M. Miyao, Appl. Phys. Lett. **96**, 082511 (2010).
[30] Y. Maeda, K. Hamaya, S. Yamada, Y. Ando, K. Yamane, and M. Miyao, Appl. Phys. Lett. **97**, 192501 (2010).
[31] S. Oki, S. Yamada, T. Murakami, M. Miyao, and K. Hamaya, Thin Solid Films **520**, 3419 (2012).
[32] K. Tanikawa, S. Oki, S. Yamada, K. Mibu, M. Miyao, and K. Hamaya, (submitted)
[33] Y. Ando, K. Hamaya, K. Kasahara, Y. Kishi, K. Ueda, K. Sawano, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **94**, 182105 (2009).
[34] Y. Ando, K. Kasahara, K. Yamane, K. Hamaya, K. Sawano, T. Kimura, and M. Miyao, Appl. Phys. Express **3**, 093001 (2010).
[35] K. Hamaya, Y. Ando, T. Sadoh, and M. Miyao, Jpn. J. Appl. Phys. **50**, 010101 (2011).
[36] Y. Ando, K. Kasahara, K. Yamane, Y. Baba, Y. Maeda, Y. Hoshi, K. Sawano, M. Miyao, and K. Hamaya, Appl. Phys. Lett. **99**, 012113 (2011).
[37] Y. Ando, Y. Maeda, K. Kasahara, S. Yamada, K. Masaki, Y. Hoshi, K. Sawano, K. Izunome, A. Sakai, M. Miyao, and K. Hamaya, Appl. Phys. Lett. **99**, 132511 (2011).
[38] Y. Ando, K. Kasahara, S. Yamada, Y. Maeda, K. Masaki, Y. Hoshi, K. Sawano, M. Miyao, and K. Hamaya, Phys. Rev. B **85**, 035320 (2012).
[39] K. Ueda, K. Hamaya, K. Yamamoto, Y. Ando, T. Sadoh, Y. Maeda, and M. Miyao, Appl. Phys. Lett. **93**, 112108 (2008).
[40] Y. Ando, K. Hamaya, K. Kasahara, K. Ueda, Y. Nozaki, T. Sadoh, Y. Maeda, K. Matsuyama, and M. Miyao, J. Appl. Phys. **105**, 07B102 (2009).
[41] K. Hamaya, H. Itoh, O. Nakatsuka, K. Ueda, K. Ya-

mamoto, M. Itakura, T. Taniyama, T. Ono, and M. Miyao, Phys. Rev. Lett. **102**, 137204 (2009).

[42] K. Kasahara, K. Yamamoto, S. Yamada, T. Murakami, K. Hamaya, K. Mibu, and M. Miyao, J. Appl. Phys. **107**, 09B105 (2010).

[43] K. Hamaya, T. Murakami, S. Yamada, K. Mibu, and M. Miyao, Phys. Rev. B **83** 144411 (2011).

[44] S. Yamada, K. Hamaya, T. Murakami, B. Varaprasad, Y. K. Takahashi, A. Rajanikanth, K. Hono, and M. Miyao, J. Appl. Phys. **109**, 07B113 (2011).

[45] S. Yamada, J. Sagar, S. Honda, L. Lari, G. Takemoto, H. Itoh, A. Hirohata, K. Mibu, M. Miyao, and K. Hamaya, Phys. Rev. B **86**, 174406 (2012).

[46] S. Yamada, K. Tanikawa, M. Miyao, and K. Hamaya, Cryst. Growth Des. **12**, 4703 (2012).

[47] K. Nakagawa, M. Miyao, and Y. Shiraki, Thin Solid Films **183**, 315 (1989).

[48] M. Miyao and K. Nakagawa, Jpn. J. Appl. Phys. **33**, 3791 (1994).

[49] S. Oki, S. Yamada, N. Hashimoto, M. Miyao, T. Kimura, and K. Hamaya, Appl. Phys. Exp. **5**, 063004 (2012).

[50] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York 1981), pp. 27-30.

[51] T. Kimura, N. Hashimoto, S. Yamada, M. Miyao, and K. Hamaya, NPG Asia Materials **4**, e9 (2012).

[52] K. Hamaya, N. Hashimoto, S. Oki, S. Yamada, M. Miyao, and T. Kimura, Phys. Rev. B **85**, 100404(R) (2012).